AMENDMENTS

IN THE SPECIFICATION

1) page 22, after the last paragraph, please add:

The invention, which provides a method for forming bonding pads of a semiconductor substrate, can be summarized as follows:

- top level interconnecting metal for interconnecting lines and top level bond pad metal for bond pads is provided, the interconnecting lines being adjacent to the top level bond pad, the interconnecting lines being adapted to ultra-small line spacing technologies, the top level metal being formed selectively on an insulating film overlying the main surface of a semiconductor substrate in which a desired circuit element is being formed, the surface of the insulating film being partially exposed
- a passivation layer is deposited over the top-level metal and over the partially exposed surface of the insulating layer, the passivation layer comprising a first and a second passivation layer
- a layer of photosensitive polyimide is deposited over the passivation layer, filling keyholes between closely spaced interconnect lines, thereby eliminating any detrimental

effect caused by accumulation of semiconductor material inside the keyholes and eliminating negative effect that passivation layer imperfections have on device reliability, further preventing etching damage and damage of cracking and delamination to the surface of the passivation layer, further providing a stress buffer to the passivation layer

- the layer of photosensitive polyimide is patterned and etched thereby forming a pattern for the bonding pads
- the passivation layer is patterned and etched thereby exposing the bond pad, the patterning and etching of the passivation layer to take place after the patterning and etching of the layer of photosensitive polyimide
- the photosensitive polyimide is cured and cross-linked, the curing and cross-linking of the photosensitive polyimide to take place after the patterning and etching of the passivation layer
- the thickness of the photosensitive polyimide is within the range of between 5.0 and 9.5 μm after deposition of the photosensitive polyimide whereby shrinkage of up to 40% of the thickness can occur after curing of the layer of photosensitive polyimide, filling keyholes between closely spaced interconnect lines, thereby eliminating any

detrimental effect caused by accumulation of semiconductor material inside the keyholes and eliminating negative effect that passivation layer imperfections have on device reliability, further preventing etching damage and damage of cracking and delamination to the surface of the passivation layer, further providing a stress buffer to the passivation layer, reducing stress impact on the passivation layer, allowing for adopting planarization technology to ultra-small line spacing technology

- specifically, the top level metal for interconnecting lines and top level metal for bond pads are formed within or on top of any layer of a semiconductor device other than or in addition to the semiconductor substrate, the interconnecting lines being adjacent to the bond pads, the interconnecting lines being adapted to ultra-small line spacing technologies, or

- the top level metal for interconnecting lines and top level metal for bond pads are formed selectively on the bare main surface of a semiconductor substrate in which a desired circuit element is being formed, the interconnecting lines being adjacent to the top level metal for bond pads, the interconnecting lines being adapted to ultra-small line spacing technologies, or

- the top level metal for interconnecting lines and top level metal for bond pads are formed within or on top of any layer of a semiconductor device other than or in addition to the semiconductor substrate, or
- the top level metal for interconnecting lines and top level metal for bond pads are formed selectively on the bare main surface of a semiconductor
- further, the portion of the photosensitive polyimide that remains after completion of the patterning and etching the photosensitive polyimide is left in place to serve as a stress buffer and to provide protection against damage and extrusion of that portion of the surface of the passivation layer which is not removed by etching
- the patterning and etching the passivation layer is removing the passivation layer above and to the top metal of the bond pads, and
- additionally, a base layer of SiO_2 is created on the top surface of the substrate the base layer to be created prior to the creation of the top level metal thereby cushioning the transition of stress between the silicon substrate and the wiring layer.

Alternatively the invention, which provides method of forming planarized bonding pads within the structure of a semiconductor device, can be summarized as follows:

- a semiconductor substrate is provided, the semiconductor substrate to contain electrical circuits or other electrical functional electrical components
- a wiring layer is provided having wiring and having a plurality of bond pads having a thickness, the wiring of the wiring layer being directly connected to the bond pads in addition to being connected to the electrical circuits or other electrical functional components within the semiconductor substrate, the wiring layer being adjacent to the plurality of bond pads, the wiring of the wiring layer being adapted to ultra-small line spacing technologies, the wiring layer being formed selectively on an insulating film overlying the main surface of a semiconductor substrate in which a desired circuit element is being formed, the surface of the insulating layer being partially exposed
- a layer of top metal is deposited over the bond pads, thereby depositing bond pad metal
- a passivation layer is deposited over the wiring layer and over the bond pad metal and over the exposed surface of the insulating layer

- a layer of photosensitive polyimide is deposited over the passivation layer to a thickness within the range of between 5.0 and 9.5 μm, filling keyholes between closely spaced wiring of the wiring layer, thereby eliminating any detrimental effect caused by accumulation of semiconductor material inside the keyholes and eliminating negative effect that passivation layer imperfections have on device reliability, further preventing etching damage and damage of cracking and delamination to the surface of the passivation layer, further providing a stress buffer to the passivation layer, reducing stress impact on the passivation layer
- the layer of photosensitive polyimide is patterned and etched, thereby forming a pattern of photosensitive polyimide, the pattern being identical to the pattern of the bond pads, partially removing the photosensitive polyimide from above the surface of the bond pads
- the layer of passivation is patterned and etched, thereby removing the passivation from above the bond pads, the patterning and etching of the passivation layer to take place after the patterning and etching the layer of photosensitive polyimide, and
- the photosensitive polyimide is cured and cross-linked, thereby protecting the underlying circuitry, the curing and